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# (54) Dual Damascene process having tapered vias

(57) A process for forming a dual-damascene interconnect employs a spun-on organic layer above an interlayer dielectric having a set of apertures for vias that forms tapered regions about the apertures without penetrating the apertures. The slope of the tapered regions is transferred during the etching process to form self-aligned tapered vias. A silicon substrate (10) over which an oxide or other insulating layer (110) is first formed. A layer first level of metal interconnect (120) and a layer of $SiO_2$ (130) are formed insequent onto the structure, then an aperture (140) extending down to and stopping on metal interconnect layer is formed. Now an anti-reflective coating (ARC) layer (135) is put down and spun onto the structure. Unexpectedly, the surface tension of the ARC layer prevents the ARC material from getting into the aperture but forms a tapered rim at its edge (as illustrated). After baking the ARC layer, a layer of resist (150) is deposited, exposed, and developed to form a novel aperture (142). An non-isotropic etch using $CF_4/O_2$ chemistry as the etching gas is performed, then both the resist and ARC layer are stripped. The result is an aperture having a tapered bottom selection which, when filled with metal (147/147) and polished to become level with the top of $SiO_2$ layer produces the chemical Damascene interconnect.

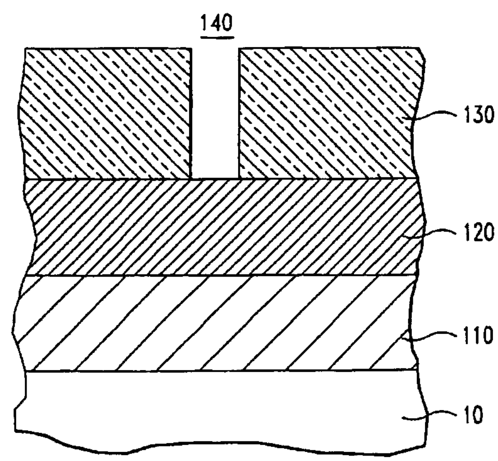


FIG. 1A

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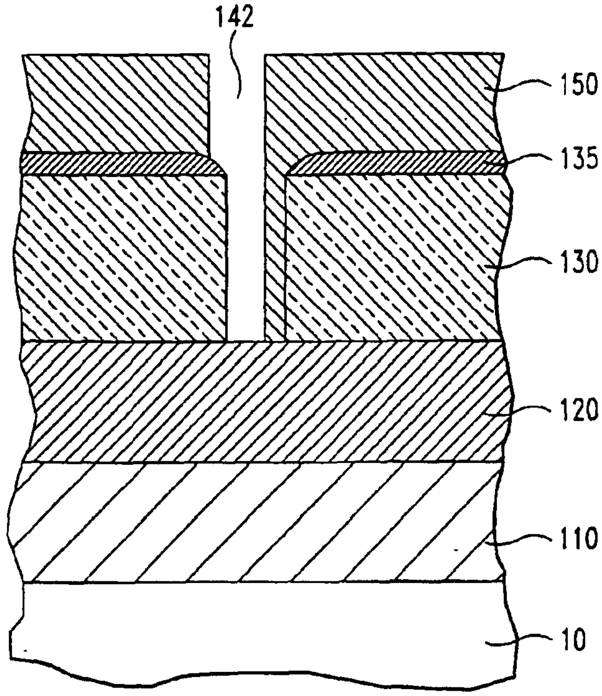


FIG. 1B

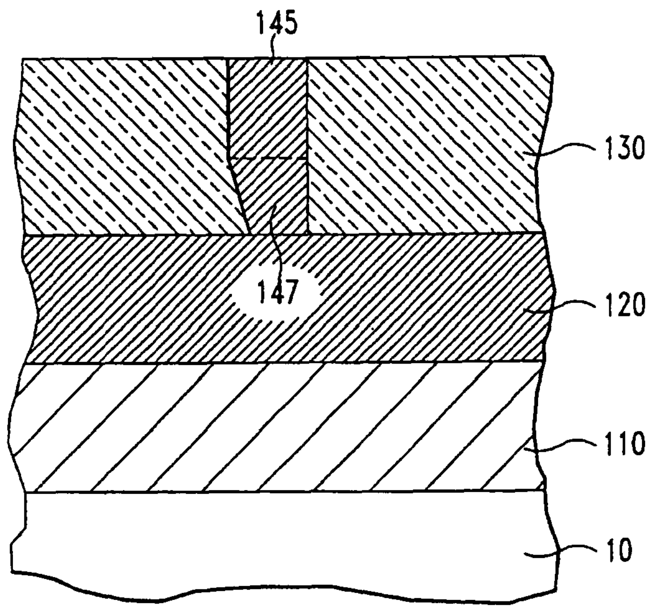


FIG. 1c

## Description

### Technical Field

The field of the invention is that of processing integrated circuits, in particular forming metal interconnections with Damascene technology (meaning a process in which the conductor is embedded in the dielectric and the tops of the conductor and the dielectric are polished to a common surface).

### Background Art

In integrated circuit processing, vertical connecting members (vias) between horizontal interconnection layers are used to improve planarity. The apertures that are formed have a high aspect ratio and are correspondingly difficult to fill without voids.

US-A- 5 173 442 illustrates a Damascene process that employs a two-level mask. US-A- 5 004 673 illustrates a Damascene process employing a mask of graded thickness at various locations.

US-A- 4 461 672 illustrates a Damascene process in which a sacrificial polysilicon layer is isotropically etched to produce a tapered opening, the taper being transferred to an underlying oxide layer. The art has long searched for a simple, low cost method of forming a Damascene-metal interconnect.

### Summary of the Invention

The invention relates to a method of forming a dual Damascene interconnect having a Damascene layer embedded within an interlayer dielectric and positioned above a via connecting to an underlying layer in which a layer of organic anti-reflective coating is deposited and spun on to a dielectric layer, and in which the surface tension of the organic layer forms a tapered rim about vias that have previously been etched into the underlying dielectric. The taper of the organic layer is then transferred into the underlying process oxide by the effect of the differential etch resistance of oxide and polymer, thereby forming a tapered via with a lower aspect ratio that is easier to fill.

### Brief Description of the Drawings

Figures 1a through 1c illustrate a portion of an integrated circuit at various steps of the invention.

Figure 2 illustrates a technique in the prior art.

Figure 3 illustrates a portion of an integrated circuit showing in cross-section Damascene interconnections formed according to the invention.

Figures 4 and 5 illustrate the effect of misalignment between the via and the Damascene layer.

### Detailed Description of the Invention

Referring now to Fig. 1A, there is shown a substrate 10 over which an oxide or other insulating layer 110 is formed. A first level of metal (illustratively aluminum) interconnect 120 extends from left to right in the drawing. Above layer 120, a layer of oxide ($SiO_2$) 130 having a nominal thickness of between 200nm and 300nm has been put down and etched in a standard, non-isotropic etch process using $CF_4/O_2$ chemistry as the etchant to form aperture 140 extending down to and stopping on metal 120.

In Fig. 1B, the same location is shown after a layer -of anti-reflective coating (ARC) 135, such as that illustrated in U.S. Patent 5,294,680, has been put down and spun on to a nominal thickness of 90nm. Those skilled in the art would expect that the spinning process and deposition process would result in the penetration of aperture 140 by some of layer 135, but it has been found that this does not happen. In a layer according to the invention, the surface tension of layer 135 both prevents the material in the layer from getting into aperture 140, and also serves to form a tapered rim from the edge of aperture 140 to the average level of layer 135. The tapered region about the via has a slope that will be referred to as the ARC slope. After baking layer 135 at 225°C, a layer of resist 150 is deposited, exposed, and developed to form aperture 142.

Aperture 142 is shown as misaligned in order to highlight an aspect of the invention that will be discussed with respect to Fig 4. As is conventional, aperture 140 extends perpendicular to the plane of the paper by a much smaller amount than the damascene conductor, which must reach another node of the circuit that may be far away.

In Fig. 1C, the result of a non-isotropic etch using $CF_4/O_2$ chemistry as an etching gas in an insulator etching system, has been performed and resist 150 and ARC layer 135 have been stripped. The result is an aperture having a tapered bottom section that has been filled with metal and polished to become level with the top of oxide 130. The via is designated with the numeral 147 and the Damascene interconnect is denoted with the numeral 145. Interconnect 145 extends perpendicular to the plane of the paper to connect with some other node in the circuit. The taper of the via is shown at a steeper angle (having a larger via slope) than the taper of ARC 135 because the taper is magnified by the differential effect of the etchant on the ARC and on the oxide. In the example illustrated, the etch resistance is in the ratio of 3:1 so the oxide etches much faster at the edge of aperture 142 than it does where the ARC is thicker. The amount of taper can be adjusted by modifying the selectivity of the etch process as is known in the art. For example, the parameters of the plasma, the etchant chemistry and/or the ARC composition may be changed.

The advantages of a tapered via - that of a lower

aspect ratio to be filled by the subsequent metal deposition process - are well known and need not be repeated here.

In the embodiment illustrated, aperture 140 had a nominal width of 300nm and layer 135 illustratively a conventional bottom anti-reflective layer (BARL) had a thickness of 90nm. The BARL layer will form droplets of a characteristic size dependent on at least the surface tension of the material and the wettability of the surface. If the characteristic size is considerably smaller than the aperture, it will be relatively easy for droplets to penetrate the aperture. Those skilled in the art will readily be able to select coating of appropriate viscosity and surface tension to avoid penetration and to achieve a desired taper in a rim about aperture 140. As noted above, the taper of the via can be adjusted by altering the selectivity of the etching parameters in a conventional manner. The nominal thickness of oxide 130 was 900nm and the nominal thickness of damascene interconnect 145 was 500nm. The wafer was degassed at 350°C for one minute in order to reduce later outgassing in the high temperature Al deposition step. A layer of 20nm of Ti was deposited through a collimator having an aspect ratio of 1.5 in order to provide better fill of the high aspect via. The wafer was cooled for one minute by a flow of Ar to prevent agglomeration of the Ti layer. The wafer is transferred to a module of the tool where 150nm of Al are deposited at 50°C using a collimator having an aspect ratio of 1.5, followed by the deposition of 550nm of Al at a temperature greater than 450°C and preferably 525°C without the use of a collimator, after which the wafer is actively cooled in a separate cooling station. The use of a hot-Al deposition technique produces a mean Al grain size of about 0.2μm, so that there are few grain boundaries in a wire having a nominal dimension of 0.25μm. Thus, Al atoms can migrate only by interfacial or lattice diffusion, which is slower than grain boundary diffusion. Moreover, the short cooling allows the Cu in the Al alloy to stay in solution, where it can readily replenish depleted boundaries.

Referring now to Fig. 2, there is shown a similar portion of a circuit part way through a process according to the art. An aperture 140' has been formed by a two-step etching process. In the first step, the same as the inventive process, an aperture has been formed all the way to the surface of metal 120. In a second step, a wider aperture has been defined and a second reactive ion etching step has formed a straight-sided upper area of aperture 140'. This etching is effective, but suffers from the disadvantage that the aperture to be filled in the following metal deposition step has a high aspect ratio and therefore is susceptible to the formation of voids, with the possibility of an incomplete or open circuit.

Referring now to Fig. 3, there is shown a portion of an integrated circuit illustrating the use of the invention. At the bottom of the figure, two transistors 20 and 25 have been formed in substrate 10 by conventional process. One Damascene interconnect 145 has been formed in a first layer of insulator 130 extending down through a via to make contact with source 22. Another portion of interconnect 145 has been formed to connect to source 27 of transistor 25 through another via. An interconnection line 145' out of the plane of the paper connects the two portions 145, the whole being referred to by the generic term "interconnect", referring to a conductive member that may or may not be planar and connects two or more nodes within an integrated circuit. For purposes of illustration, a second layer 130' and a second level of via 155 are shown, illustrating that the invention is suitable for use in a number of metal layers.

Referring now to Figures 4 and 5 the effect of misalignment is illustrated in top of cross sectional views. Fig 4A illustrates in a top view the misalignment shown in Fig 1 and Fig 5A illustrates correct alignment between apertures 140 and 142. The effect of misalignment is shown in Fig 4B as similar to that of Fig 1C, with the additional feature that the tapered region on the left in Fig 4B is cut off with a vertical face, while the taper on the right side is protected by photoresist 150 and is not changed. In Fig 5B, both faces of layer 135 are vertical and both sides of aperture 140 are tapered. This illustrates an additional benefit of the invention - that the apertures are self-aligned and taper is only provided where the design rules are not violated.

Preferably, the wires are isolated and planarized by a chemical-mechanical polish (CMP) using a non-corrosive slurry, in order to eliminate any damage to the interconnects during the CMP operation. The process has been disclosed in the context of an antireflective coating that is used for ultraviolet exposure, but is not confined to that, and any fluid coating having a suitable surface tension may be used, regardless of its reflective properties.

## Claims

1. A method of forming an integrated circuit comprising the steps of:

   preparing a substrate;

   forming a plurality of transistors in said substrate; and

   interconnecting said plurality of transistors with interconnects to form said integrated circuit, in which said step of interconnecting comprises at least one step of forming a damascene metal interconnect in a first dielectric layer, said damascene metal interconnect connecting nodes in said circuit lying below said first dielectric layer by means of conductive vias extending downwardly from said damascene metal interconnect to a lower electrical member, and in which said vias and said damascene metal in-

terconnect are formed by the steps of:

etching a set of first apertures having substantially vertical sides in contact areas of said first dielectric layer;

spinning on a layer of fluid coating on said first dielectric layer, whereby said layer of fluid coating has a set of tapered regions about said set of first apertures with a fluid coating taper extending from rims of said apertures to a nominal fluid coating surface and having a fluid coating slope;

depositing a layer of photoresist above said layer of fluid coating;

forming a set of second apertures in said layer of photoresist above said set of first apertures and said set of tapered regions;

etching through said second apertures with a non-isotropic etchant that attacks said first dielectric layer preferentially to said fluid coating, whereby said first apertures are expanded laterally and said sides of said second apertures are tapered with a taper having a via slope greater in magnitude than said fluid coating slope.

**2.** A method according to claim 1, in which said set of first apertures extend partially through said first dielectric layer.

**3.** A method according to claim 2, further comprising the steps of performing a collimated deposition of a first layer of metal in said set of second apertures, followed by a non-collimated deposition of a second layer of metal to fill said set of second apertures.

**4.** A method according to claim 3, in which said step of non-collimated deposition is performed at a temperature greater than 450°C.

**5.** A method according to claim 1, in which said set of first apertures extend through said first dielectric layer.

**6.** A method according to claim 5, further comprising the steps of performing a collimated deposition of a first layer of metal in said set of second apertures, followed by a non-collimated deposition of a second layer of metal to fill said set of second apertures.

**7.** A method according to claim 6, in which said step of non-collimated deposition is performed at a temperature greater than 450°C.

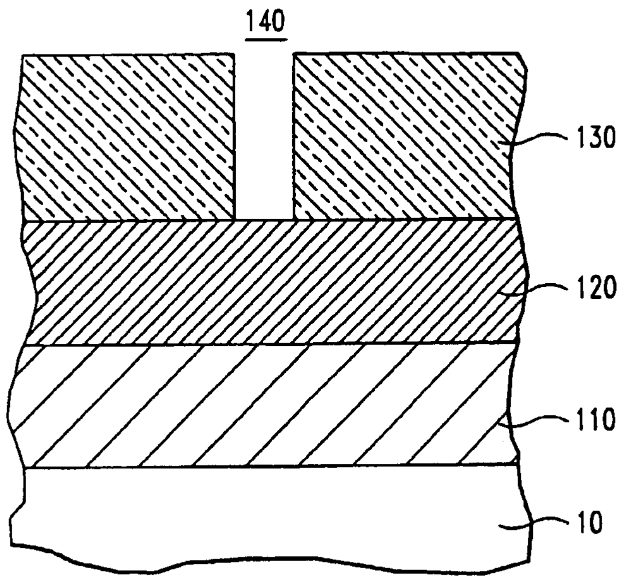


FIG. 1A

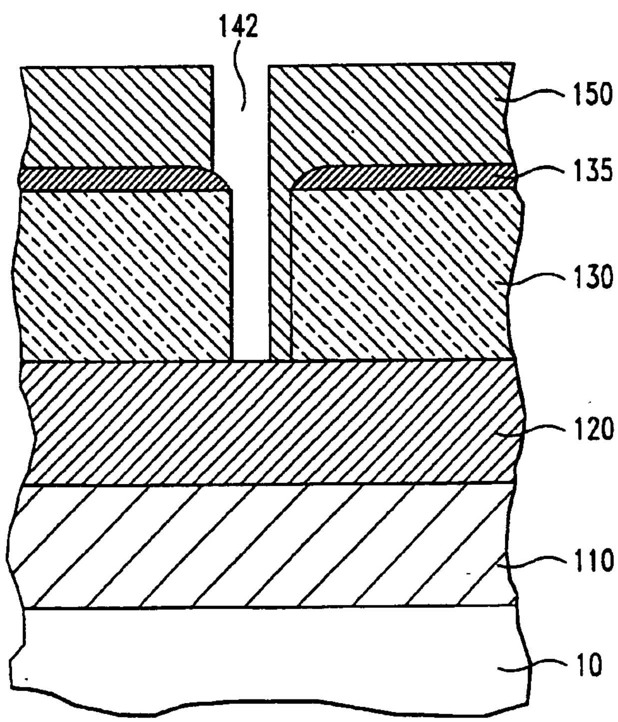


FIG. 1B

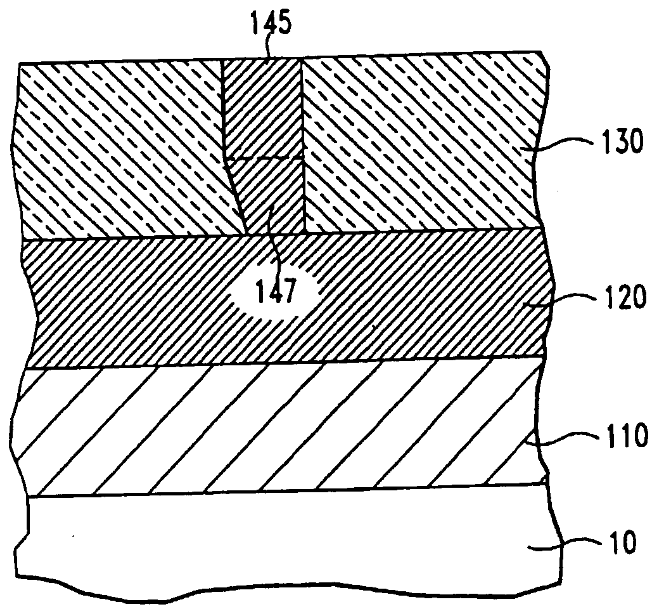


FIG. 1c

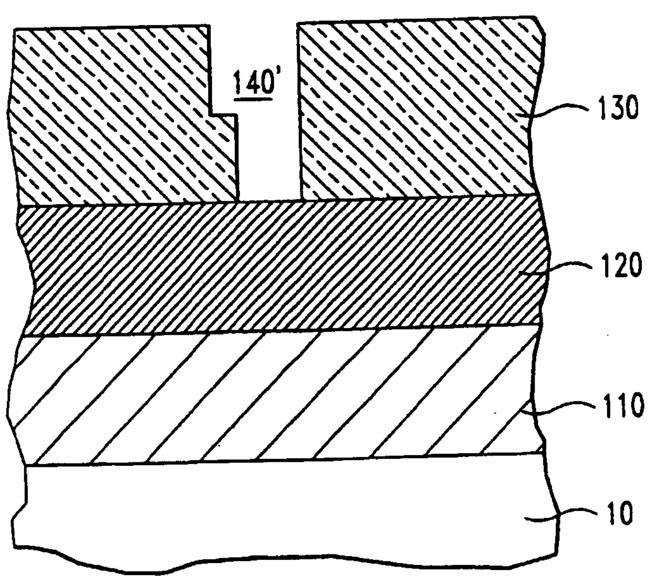


FIG. 2 PRIOR ART

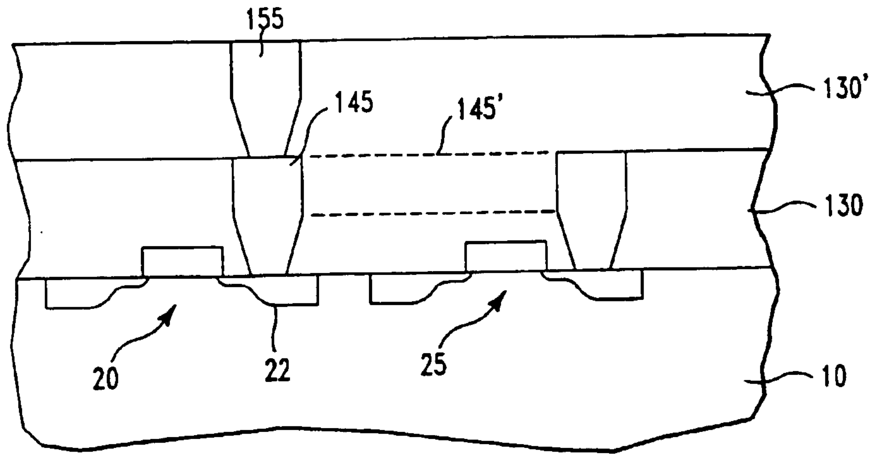


FIG. 3

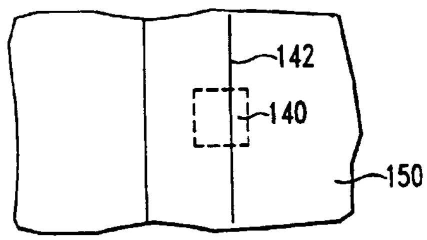


FIG. 4A

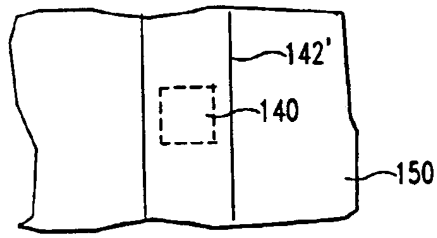


FIG. 5A

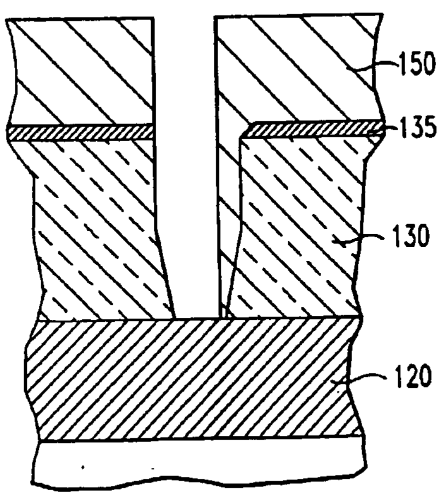


FIG. 4B

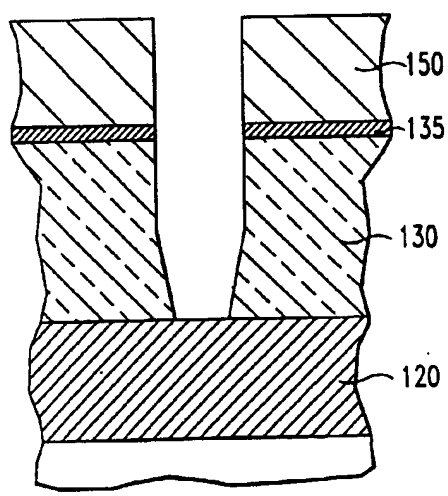


FIG. 5B